IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Noriyasu Sakai et al. Art Unit : 2812
Serial No. : 10/667,681 Examiner : Scott B Geyer
Filed : September 22, 2003
Title : METHOD FOR MANUFACTURING CIRCUIT DEVICES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. §1.131

I, Yusuke Igarashi, declare as follows:

1. I have read and understood this declaration.

2. I am one of the inventors named in the U.S. Patent Application identified above.

3. I currently am employed by Sanyo Electric Co., Ltd., the assignee of this application and I was employed by Sanyo Electric Co., Ltd. at the time the invention was made.

4. I have read and understood the patent specification identified above, including the drawings and pending claims 1-14.

5. I understand that the pending specification has a filing date of September 22, 2003, and claims priority from a Japanese patent application whose filing date is September 27, 2002.

6. I understand that pending claims 1, 2, and 11-13 were rejected as unpatentable over U.S. Patent No. 6,767,767 (Hayashida et al) in view of U.S. Patent No. 5,924,190 (Lee et al.).

7. I understand that the Hayashida et al. patent is based on an application whose U.S. filing date is July 16, 2002.

8. The subject matter of claims 1, 2 and 11-13 was invented by me and my co-inventors in Japan prior to July 16, 2002.

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

January 20, 2006
Date of Deposit

Rose Syracuse
Signature

Rose Syracuse
Typed or Printed Name of Person Signing Certificate

9. Pending claim 1 relates to a method for manufacturing circuit devices. Dependent claims 2, and 11-13 in the pending application recite various features.

10. Exhibits 1 through 4, copies of which are attached, are submitted in support of a date of invention of the subject matter of claims 1, 2 and 11-13 prior to July 16, 2002.

11. Exhibit 1 includes two pages. Exhibit 1 is a true and correct copy of a drawing that was prepared under my direction, except that a date on the second page has been redacted. The redacted date is prior to July 16, 2002.

Exhibit 1 includes information describing subject matter that was incorporated into the pending patent application.

Exhibit 1 is discussed in more detail below.

12. Exhibit 2 includes one page. Exhibit 2 is a true and correct copy of a drawing specification that was prepared under my direction, except that several dates have been redacted. The redacted dates are prior to July 16, 2002.

Exhibit 2 includes information describing subject matter that was incorporated into the pending patent application

Exhibit 2 is discussed in more detail below.

13. Exhibit 3 includes one page. Exhibit 3 is a true and correct copy of a drawing that was prepared under my direction, except that a date has been redacted. The redacted date is prior to July 16, 2002.

Exhibit 3 includes information describing subject matter that was incorporated into the pending patent application.

Exhibit 3 is discussed in more detail below.

14. Exhibit 4 includes one page. Exhibit 4 is a true and correct copy of a drawing that was prepared under my direction, except that a date has been redacted. The redacted date is prior to July 16, 2002.

Exhibit 4 includes information describing subject matter that was incorporated into the pending patent application.

Exhibit 4 is discussed in more detail below.

15. Exhibits 5, 6, 7 and 8 are copies of Exhibits 1, 2, 3 and 4, except handwritten notations have been added to help identify relevant features.

16. Pending claim 1 recites a method for manufacturing circuit devices. The method includes forming conductive patterns on a planar body, the conductive patterns forming mounting portions for circuit elements, disposing a circuit element on at least one of the mounting portions, performing resin sealing by bringing a backface of the planar body into contact with a lower mold having air vents and by sealing a surface of the planar body with an insulating resin so that the circuit element is covered therewith and separating each mounting portion.

17. A drawing in the upper right corner of Page 2 in Exhibit 1 (and Exhibit 5) shows a lower mold that includes air vents.

18. A cross-sectional view of a planar body is shown adjacent to the lower mold.

19. Arrows are labeled "TOP" and "BTM" are provided at the top and bottom of the planar body, respectively.

20. The arrow that is labeled "BTM" indicates that the bottom of the planar body is to be brought into contact with the lower mold.

21. The illustrated lower mold can be utilized to seal the planar body with insulating resin so that circuit elements positioned on its top surface are covered with insulating resin.

22. Referring now to the drawing in the lower right corner of Exhibit 2 (and Exhibit 6), a planar body (*i.e.*, the lead frame) has a back surface that is in contact with a lower mold having vents. At the bottom of the Exhibit 2 (and Exhibit 6), the planar body (*i.e.*, the lead frame) is identified by Part Code ISB-CO-02-0011-0002.

23. Exhibit 3 (and Exhibit 7) shows the planar body (*i.e.*, the lead frame) that corresponds to the planar body (*i.e.*, the lead frame) of Exhibit 2 (and Exhibit 6). Part Code ISB-CO-02-0011-0002 is shown at the bottom right corner of Exhibit 3 (and Exhibit 7). Exhibit 3 (and Exhibit 7) also identifies Equipment Name ISB-45x219.6-R5 as corresponding to the planar body (*i.e.*, the lead frame).

24. Exhibit 4 (and Exhibit 8) shows the planar body (*i.e.*, the lead frame) that corresponds to the planar body (*i.e.*, the lead frame) shown in Exhibits 2 and 3 (and Exhibits 6 and 7). Equipment Name ISB-45x219.6-R5 is shown in the bottom right corner of Exhibit 4 (and Exhibit 8).

25. As shown in Exhibit 4 (and Exhibit 8), conductive patterns are formed on the planar body and serve as mounting portions for circuit elements. Circuit elements are disposed on the mounting portions.

26. Exhibit 4 (and Exhibit 8) also shows a pattern of dashed lines that indicate where the planar body is to be separated.

27. Pending claim 2 recites a method for manufacturing circuit devices that includes forming a block that includes a plurality of the mounting portions arranged in a matrix form. Also, performing resin sealing includes covering a plurality of circuit elements, each circuit element being coupled to one of the mounting portions.

28. Exhibit 4 (and Exhibit 8) shows a plurality of mounting portions arranged in a matrix form.

29. Performing resin sealing with the arrangement shown in the lower right drawing in Exhibit 2 (and Exhibit 6) would result in covering a plurality of circuit elements that are coupled to mounting portions that are arranged in a matrix form.

30. Pending claim 11 recites a method for manufacturing circuit devices, wherein the air vent strides over a peripheral part of the cavity and is extended from inside the cavity to an outer part of the cavity.

31. The drawing in the upper right corner of page 2 in Exhibit 1 (and Exhibit 5) shows an air vent that extends over a peripheral part of a cavity.

32. Pending claim 12 recites a method for manufacturing circuit devices, wherein bringing the backface of the planar body into contact with the lower mold having air vents comprises bringing the backface of the planar body into contact with at least one of the air vents.

33. The drawings on page 2 of Exhibit 1 (and Exhibit 5) indicate that the bottom face of the planar body (*i.e.*, lead frame) is brought into contact with at least one of the air vents in the lower mold.

34. Pending claim 13 recites a method for manufacturing circuit devices wherein bringing the backface of the planar body into contact with at least one of the air vents comprises enabling the release of air through the air vent from between the planar body and the lower mold.

35. The arrangement shown on page 2 of Exhibit 1 (and Exhibit 5) enables air to be released through the air vent from between the planar body and the lower mold.

36. The application from which the present application claims priority was filed in Japan on September 27, 2002, less than three months after the U.S. filing date for the Hayashida et al. patent and indicates that my co-inventors and I diligently pursued reducing the subject matter to practice from at least a date just before July 16, 2002.

37. I hereby declare that all statements made herein are of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Dated: Jan. 12, 2006 Signed: Yusuke Igarashi
Yusuke Igarashi

30262689.doc

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Serial No.	: 10/667,681	Examiner	: Scott B Geyer
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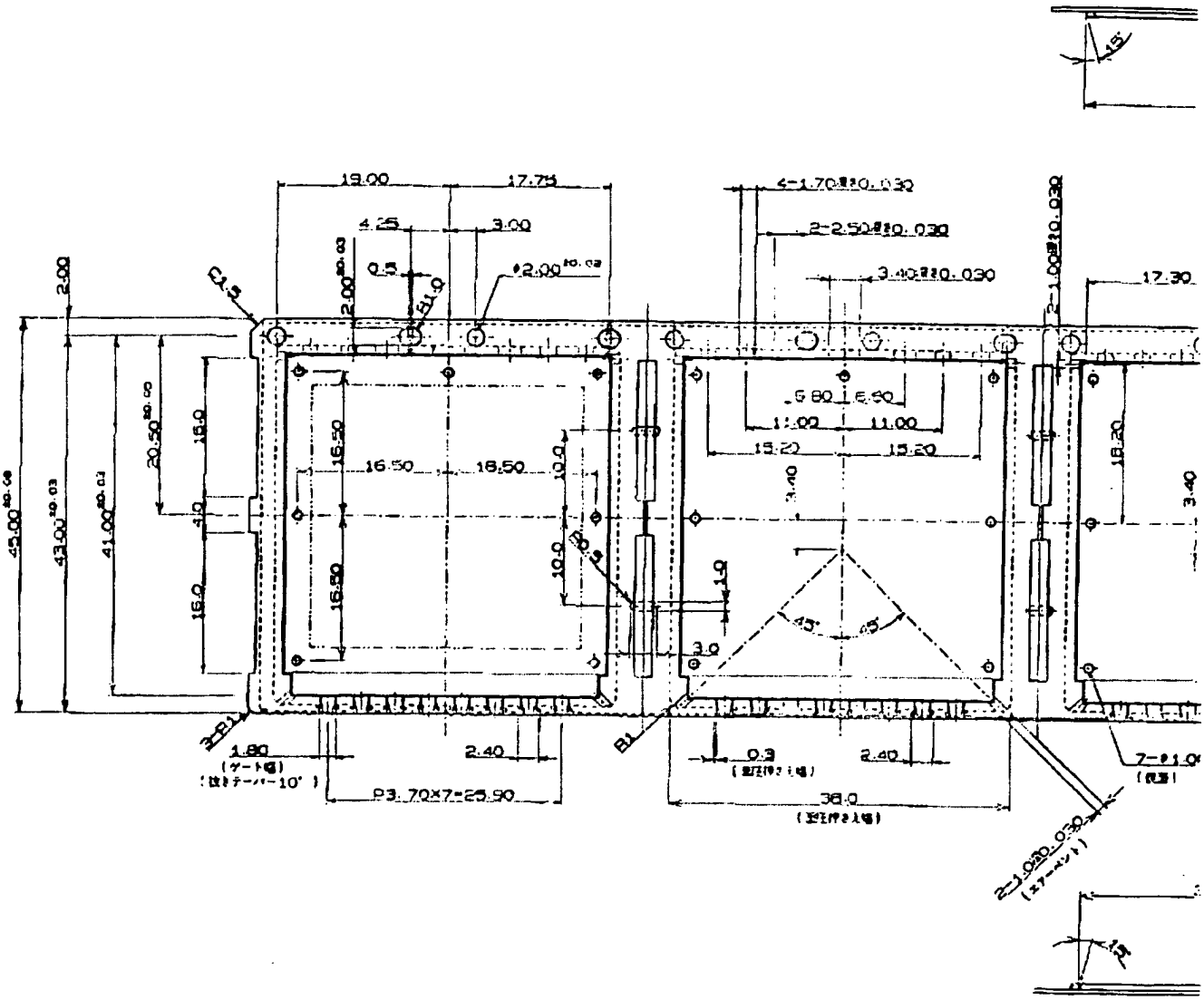
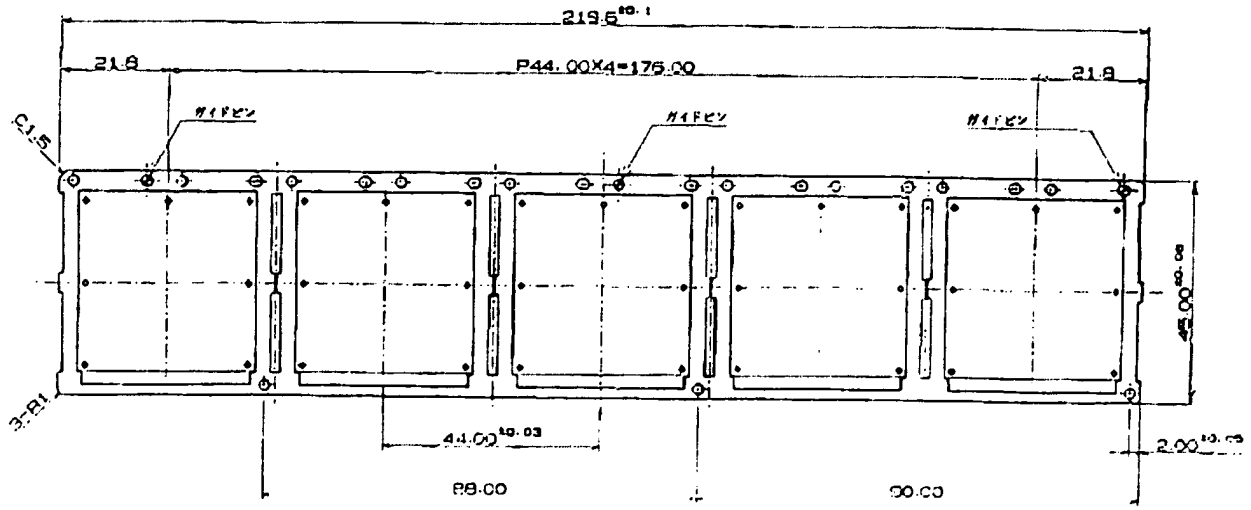
YUSUKE IGARASHI, DECLARATION UNDER 37 C.F.R. §1.131

EXHIBIT 1 (TWO PAGES)

一般寸法精度
0°±0.5　0.0°±0.1　0.00°±0.05　0.000°±0.001





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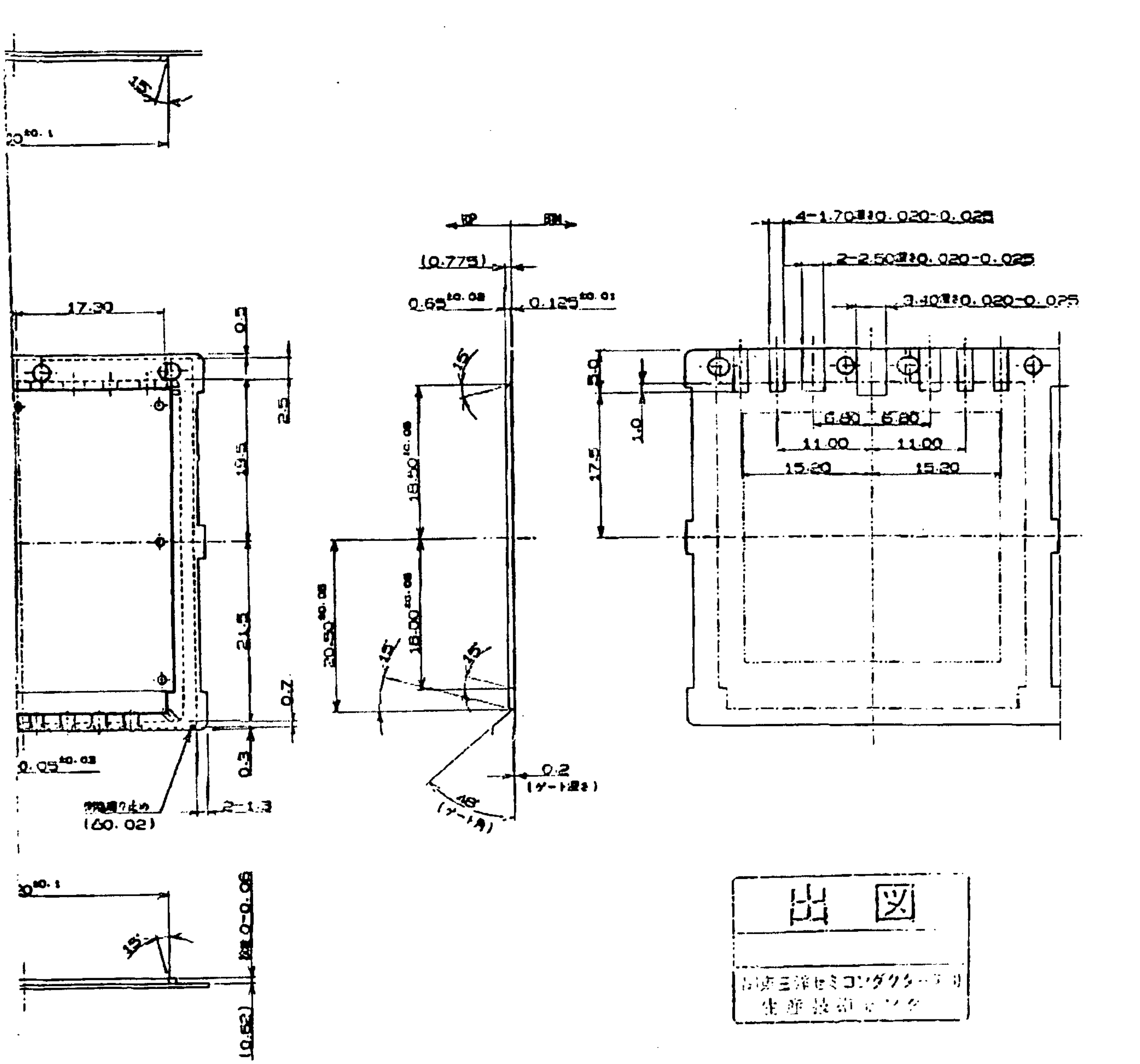

リードフレーム
　名称／図番　：
　材質　：
　[illegible]　：

樹脂
　メーカー　：
　タイプ　：
　タブレット重量　：　g
　タブレット直径　：
　タブレット高さ　：　mm
　比重　：
　成形収縮率　：　%（メーカー値）
　圧縮率　：　%以上

製品規格
　モールドとL／Fのズレ　：X　：　MAX
　　　　　　　　　　　　　Y　：　mm MAX
　　※リードフレームの寸法公差は含まない
　モールド表面　：TOP　：　面粗度　μ　mRz
　E−PIN表面　：鏡　面
　指示無きコーナーR　：R0　MAX（放電自然R）

備考
　1）リードフレームの寸法公差は、成形前の寸法を示す

承認	検図	△ △ △	製品名 G−CUBE	シリアルNo. MPE041
			名称	
設計 堀江	製図 堀江	材料仕様 T×L×W − × − × − 関東三洋セミコンダクターズ株式会社 生産技術センター	品名 製品図（　　仕様）	
			尺度 2/1	図番

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EXHIBIT 2 (ONE PAGE)

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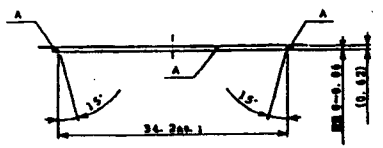

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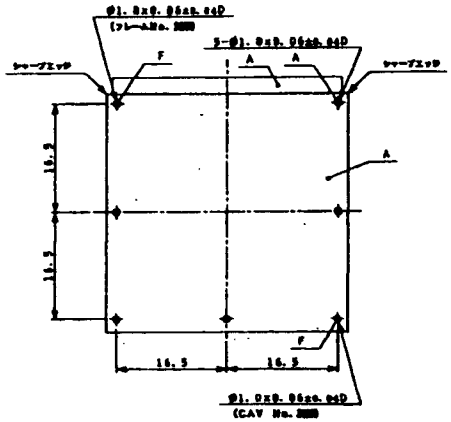

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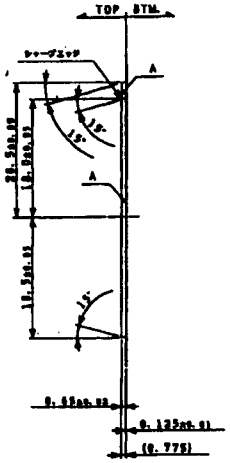

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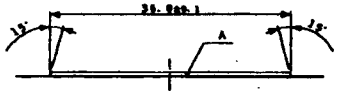

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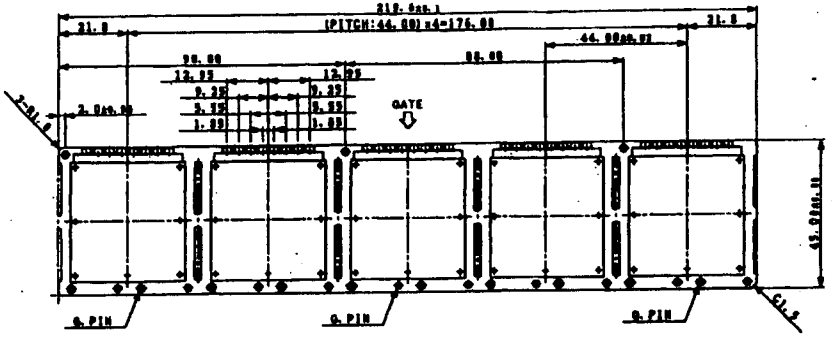

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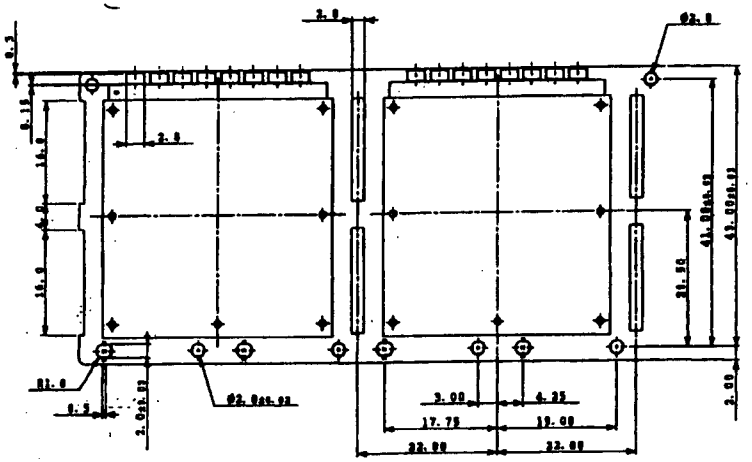

PACKAGE SURFACE

LABEL NAME	SURFACE (μmRz)
A	±±2
B	
C	
D	
E	
F	POLISH

GENERAL TOLERANCE

DRAWING NAME	TOLERANCES	ANGLES
LEAD FRAME	±0.05	-
PACKAGE	±0.1	±1.0°

DRAWING TO BE REFERED

LEAD FRAME	ISS-CO-02-0011-0002
PACKAGE	ISS-CO-02-0011-0002

MATERIAL	NAME
	MQAP PACKAGE DRAWING DCA-1560

SCALE	UNIT	REVISED	UNIT-TYPE	INDEX	PART NO.	REV. NO.
			M2MD01-001	0011	06018111	00

APIC YAMADA CORPORATION

MCAD2000

Attorney's Docket No.: 14225-022001 / F1030476US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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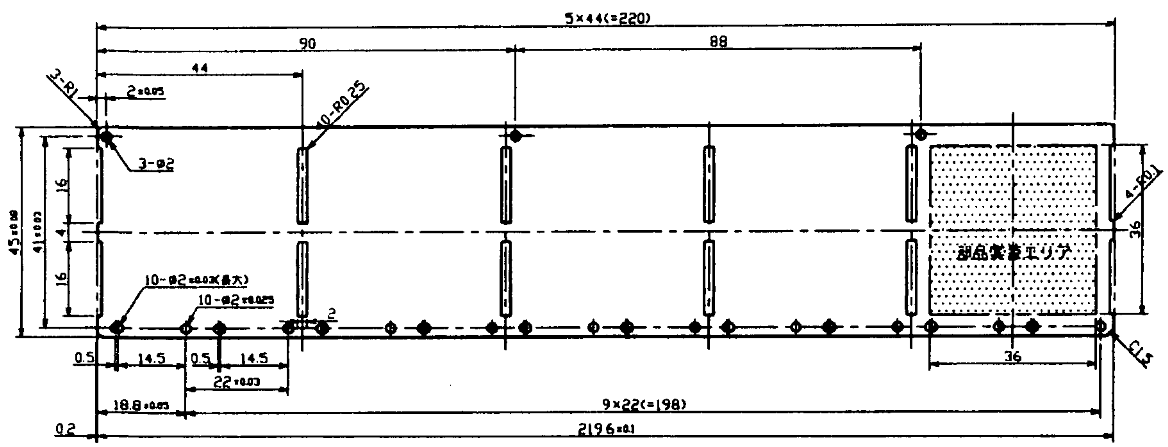
EXHIBIT 3 (ONE PAGE)



t=0.125±0.01

DIMENSIONS mm

3角法 THIRD ANGLE SYSTEM

FILE CORD

APPROVAL

CHECK

DESIGN

DRAW K. Hashima

FIRST MADE FOR (最初使用機種)

CALLED TEMP QT

CORNERS UNLESS OTHERWISE SPECIFIED, C=
RADII UNLESS OTHERWISE SPECIFIED, R=

SCALE 1/1

PART NAME (部品名)
ISBフレーム

PART No. (部品) AMOUNT (数量)

SURFACE ROUGHNESS (粗さ)

TOLERANCES UNLESS OTHERWISE SPECIFIED (寸法公差)

±	FOR	~
±	FOR	~
± 0.05	FOR	0 ~
±	FOR	ANGLES

MATERIAL SPEC (材質)
EFTEC64T-0.125t

FINISH (表面処理)
部分Agメッキ

DATE REVISIONS

PART CODE
ISB-CO-02-0011-0002

EQUIPMENT NAME
ISB-45×219.6-R5

DO NOT SCALE THIS DRAWING

関東三洋電子(株)

Attorney's Docket No.: 14225-022001 / F1030476US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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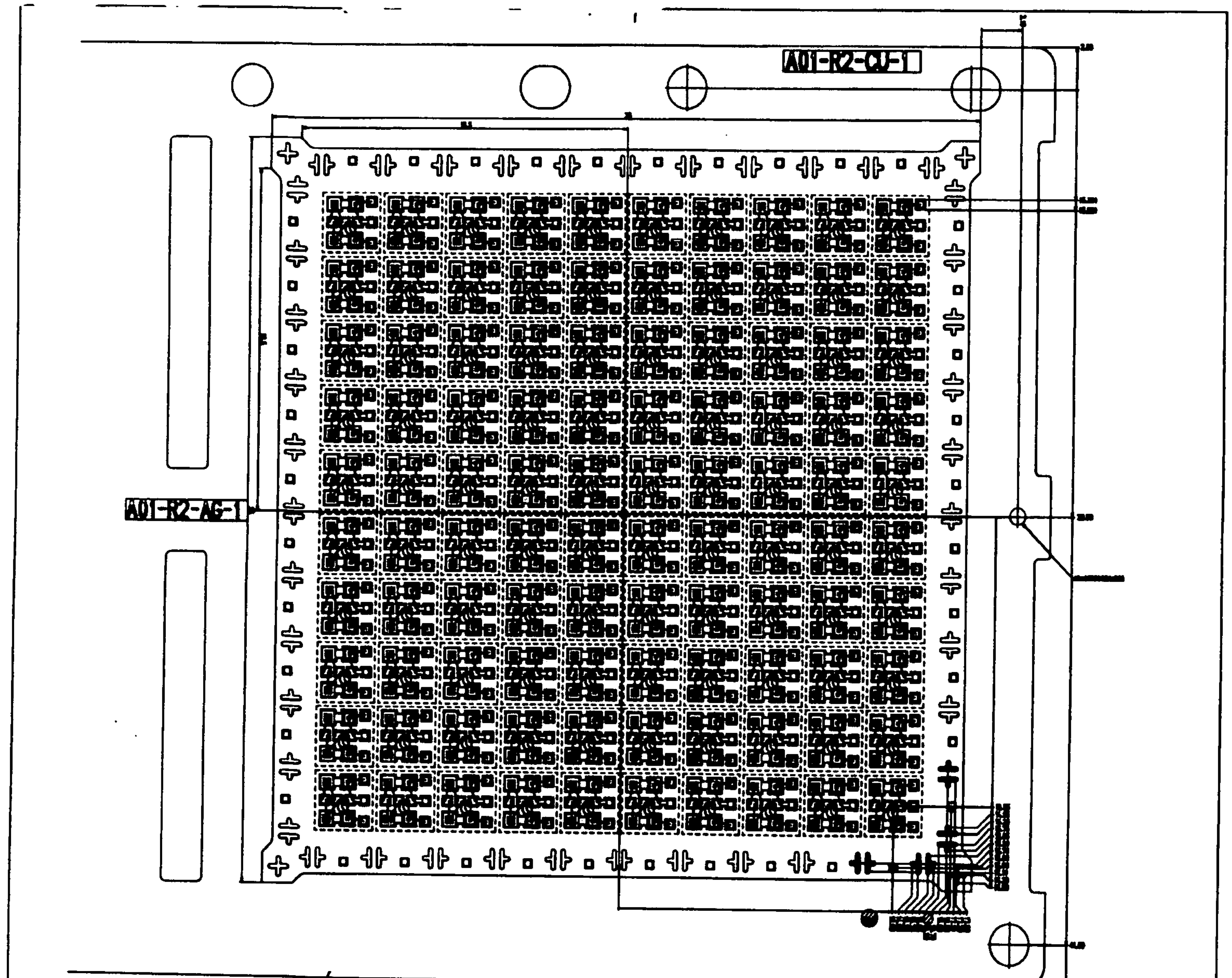
YUSUKE IGARASHI, DECLARATION UNDER 37 C.F.R. §1.131

EXHIBIT 4 (ONE PAGE)



審査	校閲	審査	校閲	修正 日付 担当者	変更内容	
				△		
				△		
				△		
				△		
				△		

材料	EFTEC64T-1/2H	TITLE	CU設計ルール	SCALE
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	メッキ厚:2.5≦10μ	ISB-A01-1	100/250μ	
	メッキ公差:±0.05	CADファイル名	外形フレーム名	
一般公差	±0.05	ISB-A01-R2Z	ISB-45x219.6-R5	

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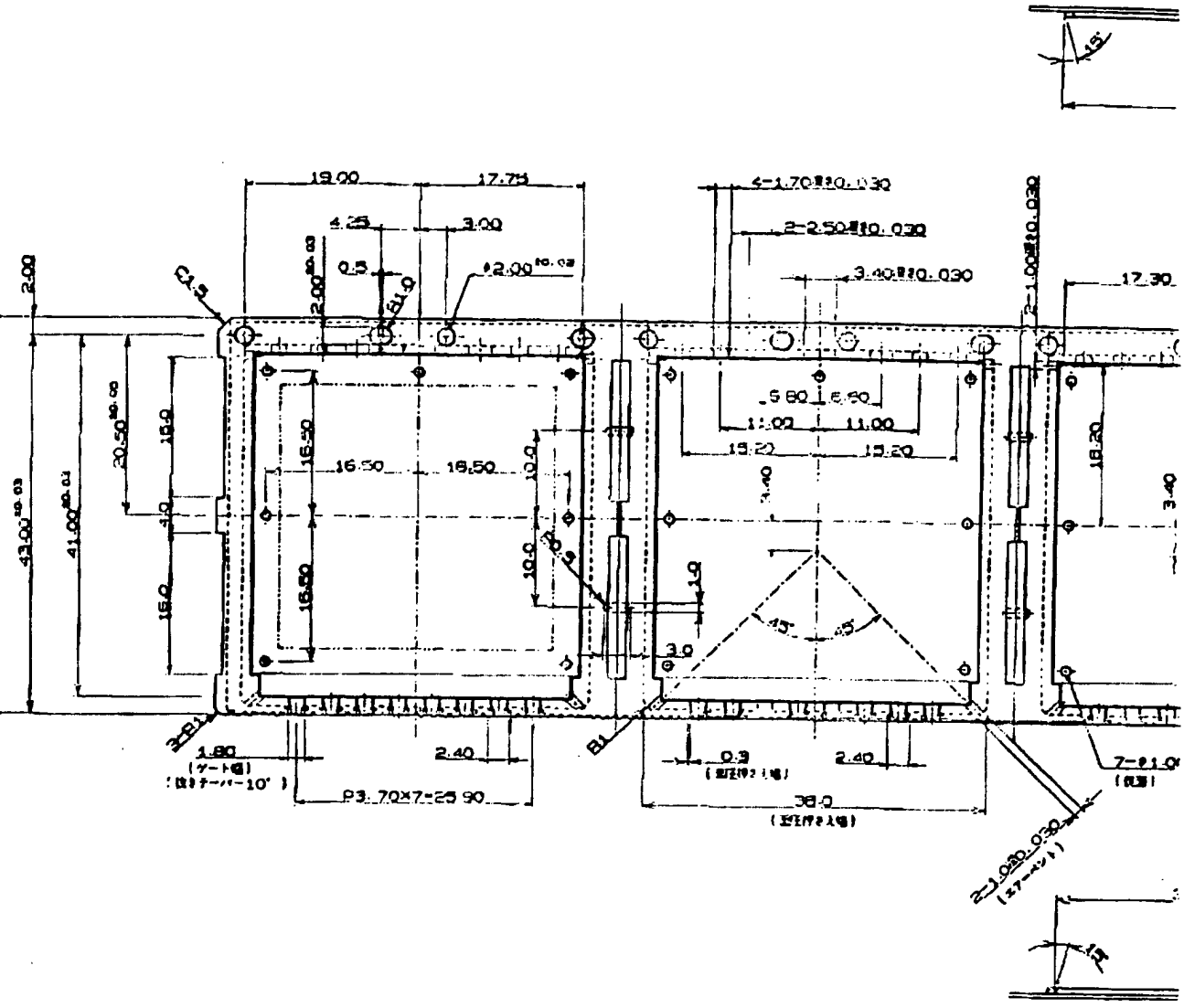
YUSUKE IGARASHI, DECLARATION UNDER 37 C.F.R. §1.131

EXHIBIT 5 (TWO PAGES)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6.50
11.00
11.00
15.20
15.20
18.20
3.40
10.0
10.0
1.0
3.0
45°
45°
2-R1
R1
1.80
(ゲート幅)
(取付テーパー10°)
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0.9
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7-φ1.0
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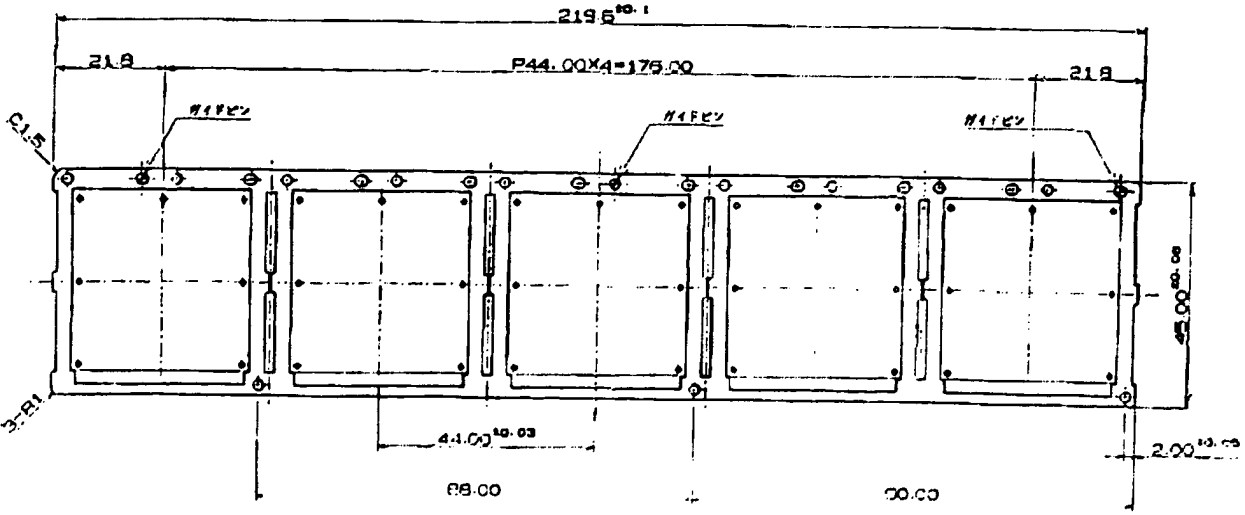
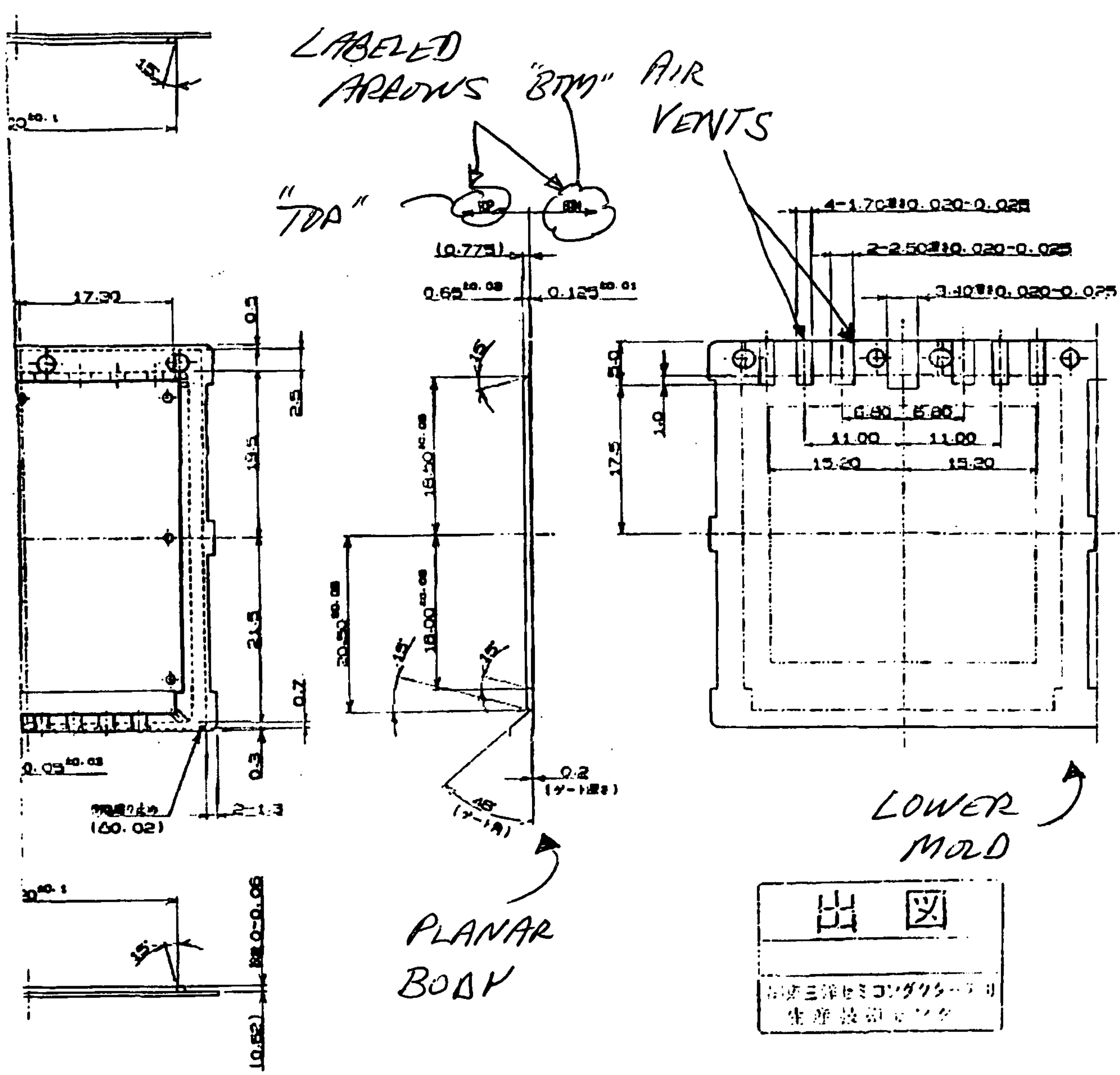
(ステージ)


219.6
21.8
P44.00×4=176.00
21.8
C1.5
ﾊﾝｶｰﾎﾞﾙﾄ
ﾊﾝｶｰﾎﾞﾙﾄ
ﾊﾝｶｰﾎﾞﾙﾄ
45.00
3-R1
44.00
2.00
88.00
90.00

(S=1/1)



リードフレーム	
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材質	:
[illegible]	:
樹脂	
メーカー	:
タイプ	:
タブレット重量	: g
タブレット直径	:
タブレット高さ	: mm
比重	:
成形収縮率	: % (メーカー値)
圧縮率	: %以上
製品規格	
モールドとL／Fのズレ	: X . MAX
	Y : mm MAX
	※リードフレームの寸法公差は含まない
モールド表面	: TOP : . 面粗度 μ mRz
E-PIN表面	: 鏡面
指示無きコーナーR	: R0 MAX (放電自然R)
備考	
1) リードフレームの寸法公差は、成形前の寸法を示す	

承認	検図	対象装置 G-CUBE	シリアルNo. MPED41
設計 堀江	製図 堀江	名称	
一般公差 T±L±W		品名 製品図(仕様)	
関東三洋セミコンダクターズ株式会社 生産技術センター		尺度 2/1	図番

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EXHIBIT 6 (ONE PAGE)

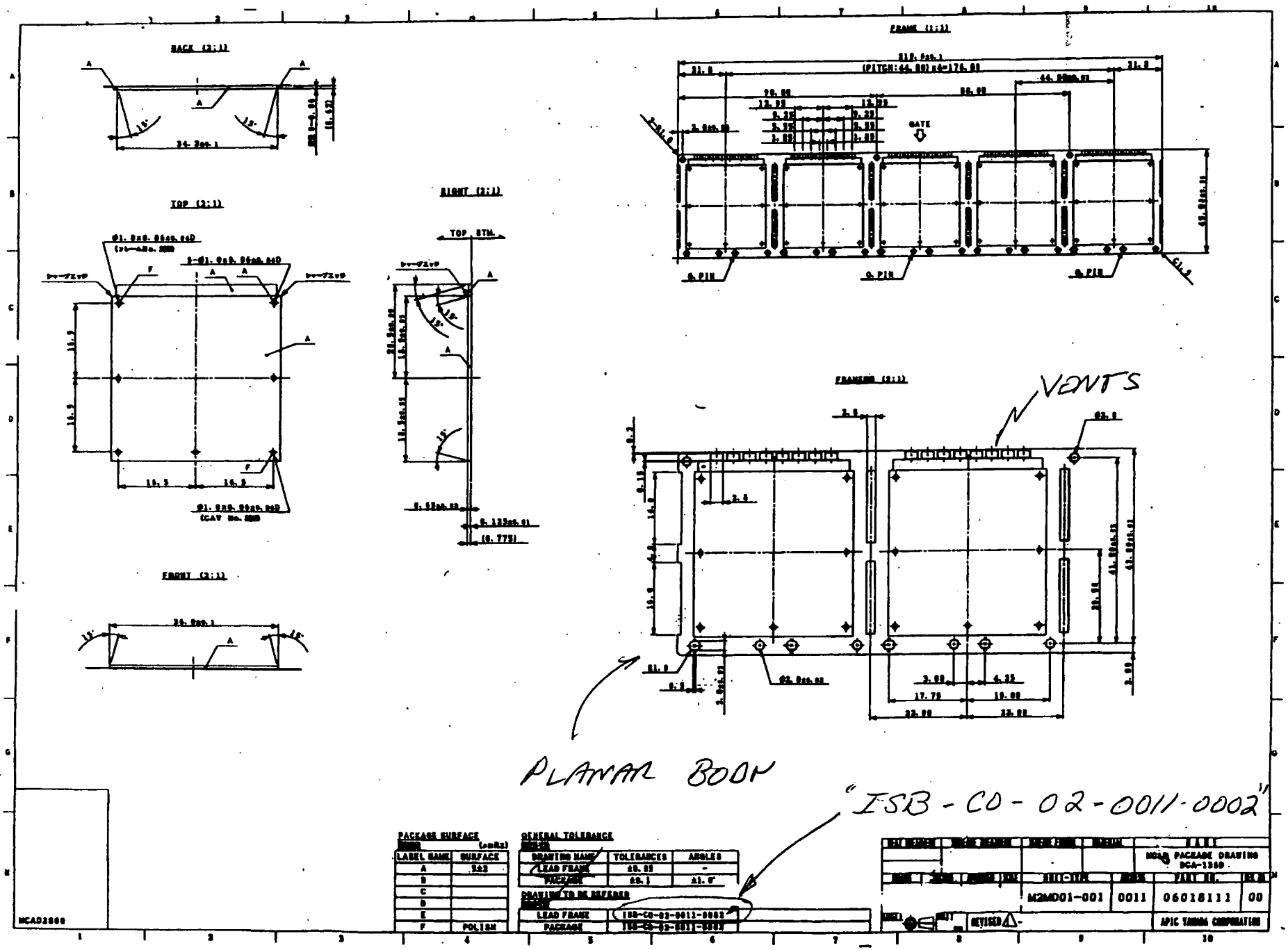
BACK (2:1)
TOP (2:1)
RIGHT (2:1)
FRONT (2:1)
FRAME (1:1)
FRAME(BB (2:1)
VENTS
PLANAR BODY
"ISB-CO-02-0011-0002"
PACKAGE SURFACE
LABEL NAME
SURFACE
A
B
C
D
E
F
POLISH
GENERAL TOLERANCE
DRAWING NAME
TOLERANCES
ANGLES
LEAD FRAME
PACKAGE
DRAWING TO BE REFERED
LEAD FRAME
PACKAGE
M2MD01-001
0011
06018111
00
REVISED
APIC YAMADA CORPORATION

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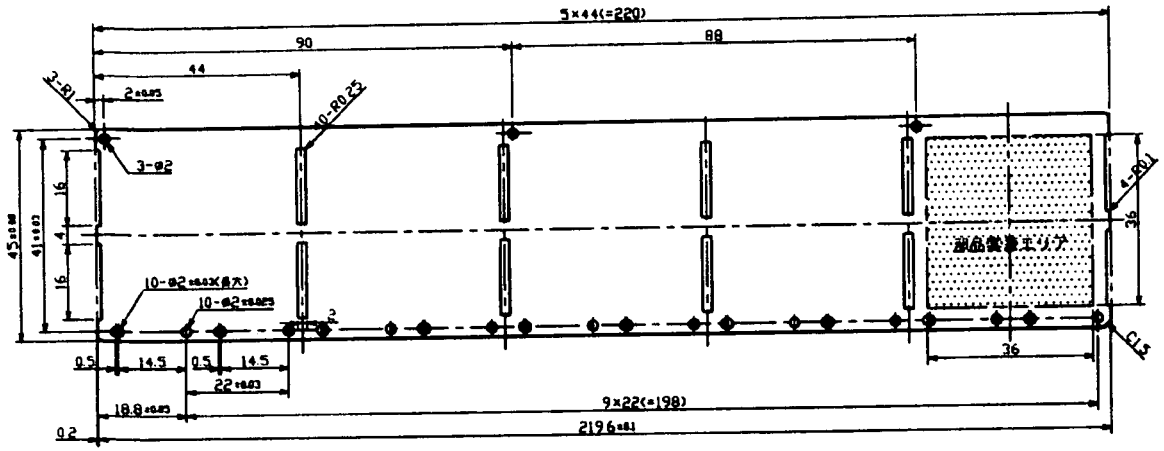
EXHIBIT 7 (ONE PAGE)



PLANAR BODY

"ISB-CO-02-0011-0002"

"ISB-45×219.6-R5"

t=0.125±0.01

DIMENSIONS	mm
	3RD THIRD ANGLE SYSTEM
FILE CORD	
APPROVAL	
CHECK	
DESIGN	
DRAW	K. Hashimoto
FIRST MADE FOR (ASSEMBLY)	
CALLED TEMP QT	

SCALE	1/1
PART NAME (JPN)	ISBフレーム
TOLERANCES UNLESS OTHERWISE SPECIFIED (ENGLISH)	
±	FOR –
±	FOR –
± 0.05	FOR 0 –
±	FOR ANGLES
MATERIAL SPEC (JPN)	EFTEC64T-0.125t
FINISH (JPN)	部分Agメッキ
PART CODE	ISB-CO-02-0011-0002
EQUIPMENT NAME	ISB-45X219.6-R5

DO NOT SCALE THIS DRAWING

DATE REVISIONS NO.

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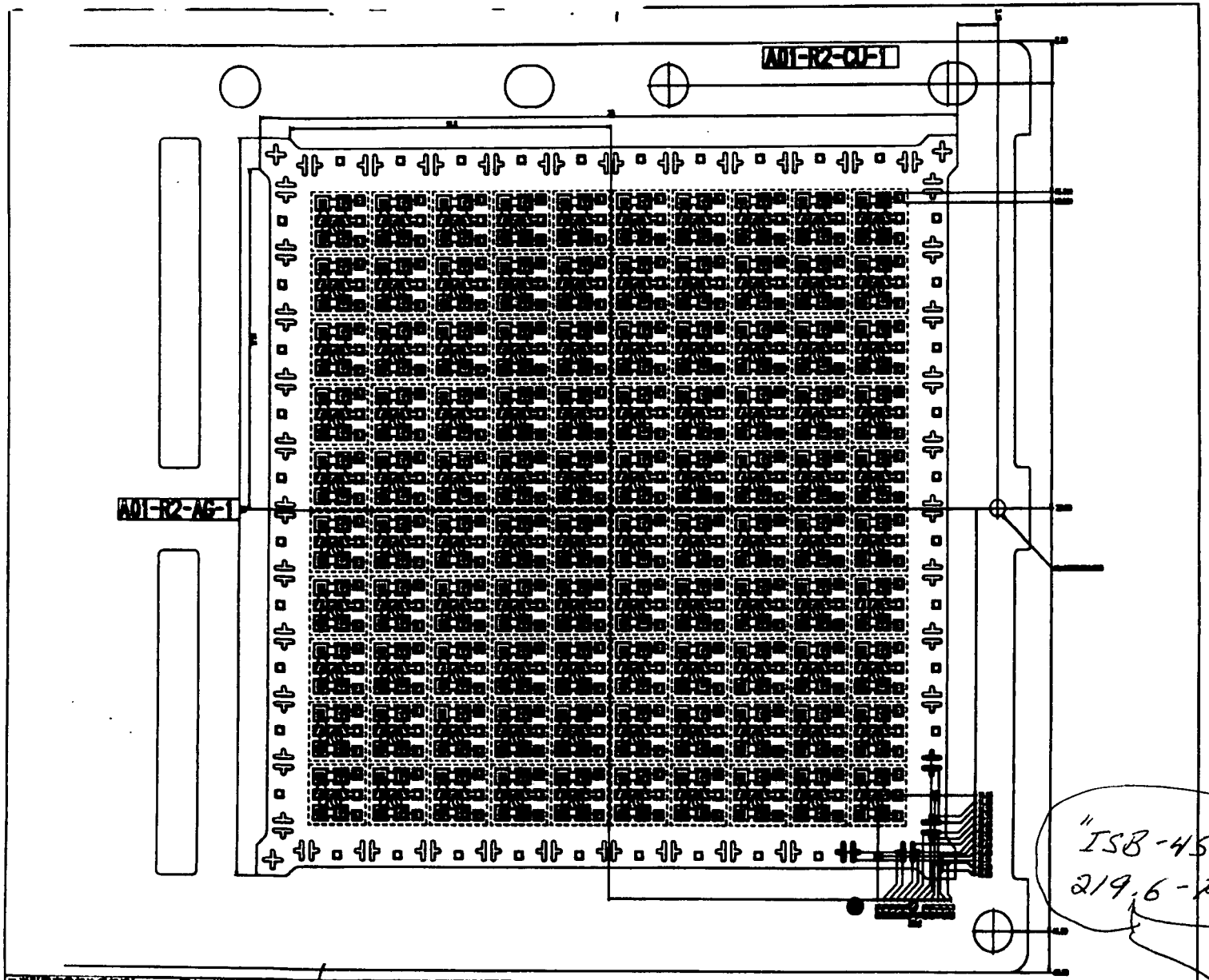
EXHIBIT 8 (ONE PAGE)



5

PLANAR BODY WITH CONDUCTIVE PATTERNS

"ISB-45x 219.6-R5"

変更	設計	変更	設計	変更	日付	承認者	変更内容
				△			
				△			
				△			
				△			
				△			

材料	EFTEC64T-1/2H	TITLE	CU層ルール(幅/間隔) SCALE
	0.125t	ISB1プロッタ用	200/150μ
	最小ドット	製品名	AG層ルール(幅/間隔)
ドット仕様	ドット径:2.5±10μ	ISB-A01-1	100/250μ 5/1
	ドット位置:±0.05	CADファイル名	外形フレーム名
一般公差	±0.05	ISB-A01-R2X	ISB-45x219.6-R5

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